## REMARKS

The Examiner objects to the Information Disclosure Statement under 37 CFR 1.98(a)(1).

The Examiner objects to the specification under 37 CFR § 1.71.

Claims 1-35 are pending in the application.

The Examiner rejects claims 23-27 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicant regards as the invention.

The Examiner rejects claims 5-17 under 35 U.S.C. §102(e) as being anticipated by Zaidi, et al. (U.S. Patent No. 6,601,126).

The Examiner rejects claims 21, 22, 34, and 35 under 35 U.S.C. §102(b) as being anticipated by Sodos (U.S. Patent No. 5,239,651).

The Examiner rejects claims 1-3, 18-20, 23-27, and 31-33 under 35 U.S.C. §103(a) as being unpatentable over Zaidi in view of Khan (U.S. Patent No. 6,163,826).

The Examiner rejects claim 4 under 35 U.S.C. §103(a) as being unpatentable over Zaidi in view of Khan and further in view of Kelley (U.S. Patent No. 6,081,863).

Applicants amend claim 23.

Claims 1-35 remain in the case.

Applicants add no new matter and request reconsideration.

### Status of the Application

Applicants respectfully request that the finality of the Office Action be withdrawn. The Examiner has submitted two new references (Zaidi and Sodos) and argued new grounds of rejection for claims 1 and 21. The new grounds of rejection were not necessitated by an amendment, as claims 1 and 21 have not been previously amended. Accordingly, Applicants submit that the finality of the instant Office Action is premature under MPEP 706.07(a), and requests that the finality of the instant Office Action be withdrawn under MPEP 706.07(d).

### Information Disclosure Statement

Applicants include a supplemental Information Disclosure Statement form 1449 listing the European Patent Application No. 0479702A2. Applicants request the Examiner consider the 0479702A2 application in evaluating the present invention.



PAGE 13/16 * RCVD AT 8/17/2004 5:31:22 PM [Eastern Daylight Time] * SVR:USPTO-EFXRP-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):06-32

**Specification Objections**

Applicants amend the specification to obviate the Examiner's objections as described in paragraph 2 of the office action.

**Claim Rejections under § 112**

Applicants amend the claim 23 to obviate the Examiner's rejections under §112.

**Claim Rejections under § 102 (e) and (b)**

The Examiner rejects claims 5-17 under 35 U.S.C. §102(e) as being anticipated by Zaidi. The Examiner rejects claims 21, 22, 34, and 35 under 35 U.S.C. §102(b) as being anticipated by Sodos. The Examiner's rejections are respectfully traversed.

Claim 5 recites *a plurality of first blocks on the chip coupled directly with the system bus, wherein...one of the first blocks is a multi-jurisdictional multi-channel general direct memory access block.*

According to the Examiner, Zaidi's M Bus 130 discloses the recited system bus. The Examiner alleges Zaidi's DMA block 134, or 138, discloses the recited multi-jurisdictional multi-channel general direct memory access block. Neither DMA block 134 or 138, however, is *coupled directly* with the M Bus 130, and therefore cannot disclose *one of the first blocks*. Zaidi, col. 4, ll. 40-44; col. 5, ll. 22-24 & 53-56; col. 6, ll. 8-10; Fig. 1. DMA block 134, or 138, further, only enables the use of a single channel and therefore does not disclose the recited multi-jurisdictional *multi-channel* general direct memory access block. Zaidi, col. 5, ll. 53-56; col. 6, ll. 8-10; Fig. 1. Since DMA block 134, or 138, is not one of the first blocks and does not disclose a multi-jurisdictional multi-channel general direct memory access block, Zaidi does not anticipate claim 5, and its corresponding dependent claims.

Claim 21 recites *granting a request by an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block to control only a system bus in an on-chip system* and *then granting a request by the mJmCGDMA block to control only an external bus in an off-chip system.* Claim 34 recites similar limitations.

According to the Examiner, Sodos's A Bus 100 discloses the recited system bus and Sodo's B Bus 160 discloses the recited external bus. The Examiner alleges Sodos's DMA controller 110 discloses the recited multi-jurisdictional multi-channel general direct memory access block. Sodos, however, does not enable DMA controller 110 to make requests for



PAGE 14/16 * RCVD AT 8/17/2004 5:31:22 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):08-32

access to either A bus 100 or B bus 160. Sodos, col. 4, ll. 26-43. Sodos, further, does not disclose either the A Bus 100 or the B Bus 160 being external to the chip. Sodos, col. 4, ll. 26-43. Since the DMA controller 110 cannot request control of either a *system bus* or an *external bus*, Sodos does not anticipate claim 21, or claim 34, and their corresponding dependent claims.

**Claim Rejections under § 103**

The Examiner rejects claims 1-3, 18-20, 23-27, and 31-33 under 35 U.S.C. §103(a) as being unpatentable over Zaidi in view of Khan. The Examiner rejects claim 4 under 35 U.S.C. §103(a) as being unpatentable over Zaidi in view of Khan and further in view of Kelley.

Claim 1 recites *a single on-chip multi-jurisdictional arbiter adapted to receive requests for ownership of the system bus and of the external bus.* The Examiner alleges that Khan's CPU bus 76 and PCI bus 82 disclose the recited system bus and external bus, respectively. The Examiner further alleges that Khan's system arbiter 26 discloses the recited *single* on-chip multi-jurisdictional arbiter. Khan's system arbiter 26, however, is comprised of two independent bus arbiters: a process bus arbiter 66 for arbitrating ownership of CPU bus 76 and a PCI bus arbiter 68 for arbitrating the ownership of PCI bus 82. Khan, col. 2, ll. 46-56; col. 5, ll. 17-19. Since process bus arbiter 66 and PCI bus arbiter 68 do not disclose *a single* on-chip multi-jurisdictional arbiter, Khan does not anticipate claim 1, and its corresponding dependent claims.

Claim 1 further recites *a single on-chip multi-jurisdictional arbiter adapted...to transmit a first grant signal to the dual first block regarding a first ownership of the external bus, and to transmit a second grant signal regarding a second ownership of the system bus to another one of the first blocks that is concurrent with the first ownership.* Claims 18, 23 and 31 recite similar limitations.

Khan does not disclose the transmitting of a second grant signal regarding second ownership of the external bus concurrent with the first ownership of the system bus since Khan only discloses the non-concurrent arbitration of multiple buses stating, "the CPU bus 76 and the PCI bus 82 are treated as one bus in the sense that a bus master must acquire ownership of both buses." Khan, Title; col. 1, ll. 35-52; col. 5, ll. 20-30. Since process bus arbiter 66 and PCI bus arbiter 68 do not disclose a single on-chip multi-jurisdictional arbiter adapted to transmit a first grant signal to the dual first block regarding a first ownership of the external bus, and to transmit a second grant signal regarding a second ownership of the system bus to another one of the first blocks that is concurrent with the first ownership, Khan



PAGE 15/16 * RCVD AT 8/17/2004 5:31:22 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):06-32

does not anticipate claim 1, or claims 18, 23 and 31, and their corresponding dependent claims.

**Claim 28-30 Rejections**

The Examiner does not specify, nor can Applicants ascertain at the time of this writing, the basis for the Examiner's rejection of claims 28-30. Applicants respectfully ask the Examiner to provide guidance.

**CONCLUSION**

Applicants request reconsideration and allowance of claims of all claims as amended. Applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

**Customer No. 20575**

Respectfully submitted,
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I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office via facsimile to the Commissioner for Patents at (703) 872-9306 on August 17, 2004.

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PAGE 16/16 * RCVD AT 8/17/2004 5:31:22 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):06-32